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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/911,035	07/23/2001	Paul C. Davis	23	3476

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EXAMINER	
VU, QUANG D	
ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 12/16/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/911,035	DAVIS, PAUL C.	
	Examiner	Art Unit	
	Quang D Vu	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10/03/02* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17 and 26-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17 and 26-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

2. Claims 1-2, 6-9, 13-16, 26-29 are rejected under 35 U.S.C. 102(e) as being anticipated by US Patent No. 6,225,674 to Lim et al.

Regarding claim 1, Lim et al. (figures 1-20) teach an integrated circuit, comprising:

a first circuit section (15) formed in a substrate (11, 14);

a second circuit section (16) formed in the substrate (11, 14), the second circuit section being spaced laterally from the first circuit section;

an isolation buried layer (12) formed under at least a portion of the first circuit section (15); and

a conductive layer (112) formed on a surface of the integrated circuit and operatively coupled to the isolation buried layer (12) at a plurality of a points spaced throughout the buried layer. It is inherent that the conductive layer (112) reducing an

effective lateral resistance of the isolation buried layer (12) to thereby increase an electrical isolation between the first (15) and second circuit (16) sections.

Regarding claim 2, Lim et al. teach a plurality of conductive plugs (33) formed in the substrate (11, 14), the plugs (33) providing a substantially low resistance path for electrically connecting the conductive layer (112) to the isolation buried layer (12).

Regarding claim 6, Lim et al. teach the isolation buried layer (12) is connected to a ground (column 8, lines 51-55).

Regarding claim 7, Lim et al. teach the conductive layer (112) is formed at least in part of metal (column 8, lines 29-30).

Regarding claim 8, Lim et al. teach a second isolation buried layer (13) formed under at least a portion of the second circuit section (16); and a second conductive layer (112) formed on a surface of the integrated circuit and operatively coupled to the second isolation buried layer (13).

It is inherent that the second conductive layer (112) reducing an effective lateral resistance of the second isolation buried layer (13).

Regarding claim 9, Lim et al. teach a plurality of conductive plugs (38) formed in the substrate (11, 14), the plugs (38) providing a substantially low resistance path for electrically connecting the second conductive layer (112) to the second isolation buried layer (13).

Regarding claim 13, Lim et al. teach the first and second conductive layers (112) are electrically connected to separate ground (column 8, lines 51-55).

Regarding claim 14, Lim et al. teach the second circuit section (16) comprises at least one bipolar transistor device, the bipolar transistor device including a collector

buried layer (20) formed in the substrate (11, 14) above the second isolation buried layer (13) (see figure 20).

Regarding claim 15, Lim et al. teach the integrated circuit is a mixed signal integrated circuit (column 9, lines 20-22); the first circuit section (15) comprises an IGFET (column 2, lines 19-20); and the second circuit section (16) comprises a bipolar transistor (column 2, lines 21-23).

It is inherent that the IGFET formed in a digital circuit section. It is inherent that the bipolar transistor formed in an analog circuit section.

Regarding claim 16, Lim et al. teach the isolation buried layer (12) has a lower resistivity than the substrate (11).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 3-5, 10-12, 17, 26-29 and 30-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,225,674 to Lim et al.

Regarding claim 3, Lim et al. differ from the claimed invention by not showing the conductive layer comprises a plurality of conductive traces, the conductive traces intersecting with and connecting to one another to form a net. It would have been obvious to one having ordinary skill in the art at the time the invention was made for the conductive layer comprises a plurality of conductive traces, the conductive traces

intersecting with and connecting to one another to form a net because it depends on the amount of noise that need to be reduced.

Regarding claim 4, Lim et al. differ from the claimed invention by not showing the net includes a plurality of holes therein, at least a portion of the first circuit section being formed in one or more holes in the net. It would have been obvious to one having ordinary skill in the art at the time the invention was made for the net includes a plurality of holes therein, at least a portion of the first circuit section being formed in one or more holes in the net because it depends on the amount of noise that need to be reduced.

Regarding claim 5, Lim et al. differ from the claimed invention by not showing the net overlays at least a portion of the first circuit section. It would have been obvious to one having ordinary skill in the art at the time the invention was made for the net overlays at least a portion of the first circuit section because it reduces noise in the first circuit section.

Regarding claim 10, Lim et al. differ from the claimed invention by not showing the second conductive layer comprises a plurality of conductive traces, the conductive traces intersecting with and connecting to one another to form a net. It would have been obvious to one having ordinary skill in the art at the time the invention was made for the conductive layer comprises a plurality of conductive traces, the conductive traces intersecting with and connecting to one another to form a net because it depends on the amount of noise that need to be reduced.

Regarding claim 11, Lim et al. differ from the claimed invention by not showing the second net includes a plurality of holes therein, wherein at least a portion of the first circuit section being formed in one or more holes in the net. It would have been obvious

to one having ordinary skill in the art at the time the invention was made for the net includes a plurality of holes therein, wherein at least a portion of the first circuit section being formed in one or more holes in the net because it depends on the amount of noise that need to be reduced.

Regarding claim 12, Lim et al. differ from the claimed invention by not showing the second net overlays at least a portion of the first circuit section. It would have been obvious to one having ordinary skill in the art at the time the invention was made for the net overlays at least a portion of the first circuit section because it reduces noise in the second circuit section.

Regarding claim 17, Lim et al. differ from the claimed invention by not showing the isolation buried layer is formed in the substrate at depth in a range from about 2 micrometers to about 5 micrometers from an upper surface of the substrate. It would have been obvious to one having ordinary skill in the art at the time of the invention was made for the isolation buried layer is formed in the substrate at depth in a range from about 2 micrometers to about 5 micrometers from an upper surface of the substrate, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Regarding claim 26, Lim et al. (figures 1-20) teach a semiconductor device, comprising:

a first circuit section (15) formed in a substrate (11, 14);

a second circuit section (16) formed in the substrate (11, 14), the second circuit section being spaced laterally from the first circuit section;

an isolation buried layer (12) formed under at least a portion of the first circuit section (15); and

a conductive layer (112) formed on a surface of the substrate and electrically coupled to the isolation buried layer (12) at a plurality of a points spaced throughout the buried layer.

It is inherent that the conductive layer (112) reducing an effective lateral resistance of the isolation buried layer (12) to thereby increase an electrical isolation between the first and second circuit sections (15, 16).

Lim et al. do not teach a semiconductor device formed on a semiconductor wafer. It would have been obvious to one having ordinary skill in the art at the time the invention was made for a semiconductor device formed on a semiconductor wafer because the semiconductor wafer is a well known substance for manufacturing semiconductor device.

Regarding claim 27, Lim et al. teach a plurality of conductive plugs (33) formed in the substrate (11, 14), the plugs (33) providing a substantially low resistance path for electrically connecting the conductive layer (112) to the isolation buried layer (12).

Regarding claim 28, Lim et al. teach a second isolation buried layer (13) formed under at least a portion of the second circuit section (16); and a second conductive layer (112) formed on a surface of the substrate and electrically coupled to the second isolation buried layer (13).

It is inherent that the second conductive layer (112) reducing an effective lateral resistance of the second isolation buried layer (13).

Regarding claim 29, Lim et al. teach a plurality of conductive plugs (38) formed in the substrate (11, 14), the plugs (38) providing a substantially low resistance path for electrically connecting the second conductive layer (112) to the second isolation buried layer (13).

Regarding claim 30, Lim et al. teach an integrated circuit, comprising:

a first circuit section (15) formed in a substrate (11, 14);

a second circuit section (16) formed in the substrate (11, 14), the second circuit section being spaced laterally from the first circuit section;

an isolation buried layer (12) formed under at least a portion of the first circuit section (15); and

a conductive layer (112) formed on a surface of the integrated circuit and operatively coupled to the isolation buried layer (12). It is inherent that the conductive layer (112) reducing an effective lateral resistance of the isolation buried layer (12).

Lim et al. differ from the claimed invention by not showing the conductive layer comprises a plurality of conductive traces, the conductive traces intersecting with and connecting to one another to form a net. It would have been obvious to one having ordinary skill in the art at the time the invention was made for the conductive layer comprises a plurality of conductive traces, the conductive traces intersecting with and connecting to one another to form a net because it depends on the amount of noise that need to be reduced.

Regarding claim 31, Lim et al. teach an integrated circuit, comprising

a first circuit section (15) formed in a substrate (11, 14);

a second circuit section (16) formed in the substrate (11, 14), the second circuit section being spaced laterally from the first circuit section;

a first isolation buried layer (12) formed under at least a portion of the first circuit section (15);

a first conductive layer (112) formed on a surface of the integrated circuit and operatively coupled to the isolation buried layer (12);

a second isolation buried layer (13) formed under at least a portion of the second circuit section (16); and

a second conductive layer (112) formed on a surface of the integrated circuit and operatively coupled to the second isolation buried layer (13).

It is inherent that the conductive layer (112) reducing an effective lateral resistance of the first isolation buried layer (12).

It is also inherent that the second conductive layer (112) reducing an effective lateral resistance of the second isolation buried layer (13).

Lim et al. differ from the claimed invention by not showing at least one of the first conductive layer and the second conductive layer comprises a plurality of conductive traces, the conductive traces intersecting with and connecting to one another to form a net. It would have been obvious to one having ordinary skill in the art at the time the invention was made for at least one of the first conductive layer and the second conductive layer comprises a plurality of conductive traces, the conductive traces intersecting with and connecting to one another to form a net because it depends on the amount of noise that need to be reduced.

Response to Arguments

Applicant's arguments with respect to claims 1-17, 26-29 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quang D Vu whose telephone number is 703-305-3826. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 703-308-2772. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

qv
December 12, 2002

Steven Loke